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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,230	02/01/2001	Hoi-Jin Lee	SAM-0192	9045

7590 05/19/2004

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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	9

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,230	LEE, HOI-JIN	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 3/26/04.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the hash logic comprising an exclusive-OR operation with various inputs of claims 4 and 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 4-5 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Panwar et al., U.S. Patent No. 5,890,008.

8. Regarding claim 1, Panwar has taught a branch predictor for a multi-processing computer able to execute multiple processes (see Col.3 line 66 – Col.4 line 49), each process having a designated process reference (see Col.10 lines 35-57), comprising:

a. A history register (BHR0 – BHR3 of Fig.5) for storing a branch history of previous sequential branch instructions (see Col.8 lines 48-55),

b. A hash logic for creating an index from a combination of a process reference of a process corresponding to a current branch instruction, an address of the current branch instruction, and the branch history (see Col.8 lines 34-47 and Col.9 lines 35-49). Here, the hash logic includes using a selected branch history register based on the current process ID (see Fig.5).

c. A branch prediction table (519 of Fig.5) for storing branch prediction reference data, and for outputting branch prediction reference data corresponding to the index created by the hash logic (see Col.8 lines 34-47),

d. An address selection circuit for selecting one of a target address known from the current branch instruction and a next instruction of the current branch instruction to generate a branch prediction address, in response to the branch prediction reference data output from the branch prediction table (see Col.8 line 56 – Col.9 line 7 and Col.9 line 50 – Col.10 line 7),

e. A branch prediction result tester (515 of Fig.5) for updating the branch history stored in the history register and the branch prediction reference data stores in the branch prediction table, in response to a real branch address and the branch prediction address according to an execution result of the current branch instruction (see Col.9 lines 18-35, 50-67).

9. Regarding claim 2, Panwar has taught the branch predictor of claim 1, wherein the branch prediction table comprises a plurality of up/down saturating counters selected by the index created by the hash logic (see Col.9 lines 58-60).

10. Regarding claim 4, Panwar has taught the branch predictor of claim 1, wherein the process reference comprises a process ID corresponding to the current branch instruction, and wherein the hash logic creates the index by performing an exclusive-OR operation on the process ID corresponding to the current branch instruction, the address of the current branch instruction, and the branch history (see Col.8 lines 34-47). Here, because the branch history register selected is based solely on the process ID of the current branch instruction (see Col.8 line 48 – Col.9 line

7), the XOR operations is inherently performed on the process ID, the address of the current branch instruction, and the branch history (via the branch history register selected by the process ID).

11. Regarding claim 5, Panwar has taught the branch predictor of claim 1, wherein the branch prediction result tester includes a comparator for determining whether a real branch address according to the execution result of the current branch instruction matches with the branch prediction address, and creates a control signal corresponding to the result (see Col.9 lines 18-35). Here, while not taught explicitly, it is inherent that some sort of signal is generated that causes the actions associated with a misprediction (pipe flush, updating of history registers and tables) to occur.

12. Regarding claim 10, Panwar has taught a method of predicting a branch address of a conditional branch instruction with reference to a branch prediction table for storing branch prediction reference data in a multi-processing computer able to execute multiple processes (see Col.3 line 66 – Col.4 line 49), each having a designated process ID (see Col.10 lines 35-57), the method comprising the steps of:

a. Creating an index to access the branch prediction table from a combination of a process ID of a process corresponding to the conditional branch instruction, an address of the conditional branch instruction, and a branch history comprising previous sequential branch instructions (see Col.8 lines 34-47 and Col.9 lines 35-49). Here, the hash logic includes using a selected branch history register based on the current process ID (see Fig.5).

b. Reading branch prediction reference data from the branch prediction table in response to the index (see Col.8 lines 34-47),

c. Selectively outputting one of a target address known from the conditional branch instruction and a next address of the conditional branch instruction in response to the branch prediction reference data (see Col.8 line 56 – Col.9 line 7 and Col.9 line 50 – Col.10 line 7),

d. Updating the branch history and the stored branch prediction reference data in the branch prediction table in response to a real branch address according to an execution result of the conditional branch instruction (see Col.9 lines 18-35, 50-67).

13. Regarding claim 11, Panwar has taught the method of claim 10, further comprising the steps of:

a. Determining whether the real branch address matches with the branch prediction address (see Col.9 lines 18-35, 50-67),

b. Changing and outputting a corrected branch address as the branch prediction address if the real branch address does not match therewith (see Col.9 lines 18-35, 50-67).

14. Regarding claim 12, Panwar has taught the method of claim 10, wherein creating the index comprises performing an exclusive-OR operation on the process ID of the process corresponding to the conditional branch instruction, the address of the conditional branch instruction, and the branch history comprising previous sequential branch instructions (see Col.8 lines 34-47). Here, because the branch history register selected is based solely on the process ID

of the current branch instruction (see Col.8 line 48 – Col.9 line 7), the XOR operations is inherently performed on the process ID, the address of the current branch instruction, and the branch history (via the branch history register selected by the process ID).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al., U.S. Patent No. 5,890,008 as applied to claims 1 and 5 above, and further in view of Talcott, U.S. Patent No. 6,272,623.

17. Regarding claim 3, Panwar has taught the branch predictor of claim 1, but has not explicitly taught wherein the history register comprises a shift register.

18. However, Talcott has taught the use of shift registers as history registers so that one bit at a time can be updated, instead of the entire register having to be rewritten for each one bit branch history update, allowing for more fine-grained control (see Talcott, Col.3 lines 44-52). One of ordinary skill in the art would have recognized that it is desirable to be able to control the writing of a register in a more fine-grained manner. Therefore, one of ordinary skill in the art would have found it obvious to modify the branch predictor of Panwar to use a shift register for the history register as taught by Talcott in order to control bitwise writing to the history register.

19. Regarding claim 6, Panwar has taught the branch predictor of claim 5, wherein the comparator generates a control signal of "taken" if the real branch address matches with the branch prediction address, and generates a control signal of "not taken" if the real branch address does not match (see Col.9 lines 18-35, 50-67), but has not explicitly taught wherein the comparator generates a control signal of logic "1" if the real branch address matches with the branch prediction address, and generates a control signal of logic "0" if the real branch address does not match.

20. However, Talcott has taught a control signal being set to logic "1" when the branch was predicted correctly, and to logic "0" when it was not so that the result can be easily used to update the history register without having to generate another signal (see Talcott, Col.3 lines 31-43). Therefore, one of ordinary skill in the art would have found it obvious to modify the branch predictor of Panwar to assign logic values of "1" and "0" to the control signal generated when a branch was predicted correctly and incorrectly, respectively, so that the history register can be easily updated with the control signals value.

21. Regarding claim 7, Panwar in view of Talcott has taught the branch predictor of claim 6, wherein the address selection circuit changes and outputs the real branch address as the branch prediction address when the control signal is logic "0" (see Panwar, Col.9 lines 50-67). Here, Panwar has taught that the address selection circuit outputs the correct branch address when the control signal is "not taken", which corresponds to the control signal being logic "0" (see above paragraphs 19-20).

22. Regarding claim 8, Panwar in view of Talcott has taught the branch predictor of claim 6, wherein the branch prediction table comprises an up/down counter, and wherein the up/down

counter increments when the control signal is logic "1", and wherein the up/down counter decrements when the control signal is logic "0" (see Panwar, Col.9 lines 59-63). Here, Panwar has taught that the up/down counter incrementing when the control signal is "taken", and decrementing when it is "not taken", which correspond to the control signal being logic "1" and logic "0", respectively (see above paragraphs 19-20).

23. Regarding claim 9, Panwar in view of Talcott has taught the branch predictor of claim 6, wherein the history register comprises a shift register, and wherein the shift register shifts the branch prediction result in a first direction by inserting the control signal (see Talcott, Col.3 lines 31-43 and above paragraphs 19-20).

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

26. Col et al., U.S. Patent No. 6,526,502, has taught a method for speculatively updating branch history using an exclusive-OR hashing function

27. D'Sa et al., U.S. Patent No. 6,715,064, has taught a method for updating branch history using transforms input to an exclusive-OR hashing function.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien

Examiner
Art Unit 2183

BJO
5/14/2004

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